In The Claims:

1. (currently amended) A method of forming a contact opening in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have first sidewall spacers, the method comprising the steps of:

forming a dielectric liner layer over the semiconductor device;

forming a dielectric layer over the dielectric liner layer, wherein an etching selectivity between the dielectric layer and the dielectric liner layer is high; and

patterning the dielectric layer using the dielectric liner layer as an etch stop and the dielectric liner layer without planarizing the dielectric layer to form a self-aligned contact window that exposes a surface of the substrate between the said first and second gates, wherein a dimension of the contact window at a top is greater than a distance between the sidewall spacers of the first gate and the second gate, and the dielectric liner layer is converted into second sidewall spacers for the first gate and the second gate.

2. (original) The method of claim 1, wherein the step of forming the dielectric liner layer includes depositing silicon nitride.

3. (original) The method of claim 1, wherein the step of forming the dielectric layer includes depositing silicon oxide.

4. (original) The method of claim 1, wherein the dielectric layer has a thickness of about 10000Å to 15000Å.

5. (original) The method of claim 1, wherein the dielectric layer comprises a dielectric layer with a good gap-filling capability and a dielectric passivation layer.

6. (currently amended) A method of forming a contact plug in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a dielectric liner layer conformal to a surface profile of the substrate and the said first and second gates;

forming a dielectric layer over the dielectric liner layer, wherein an etching selectivity between the dielectric layer and the dielectric liner layer is high;

patterning the dielectric layer using the dielectric liner layer as an etch stop and the dielectric liner layer without planarizing the dielectric layer to form a self-aligned contact window that exposes a surface of the substrate between said first and second gates, wherein a dimension of the contact window formed in the dielectric layer is greater than a distance between the sidewall spacers of the first gate and the second gate;

forming a polysilicon layer over the dielectric layer and filling the self-aligned contact window;

removing a portion of the polysilicon layer lying above the dielectric layer; and

removing a portion of the dielectric layer so that the contact plug is formed inside the self-aligned contact window.

7. (original) The method of claim 6, wherein the step of forming the dielectric liner layer includes depositing silicon nitride.

8. (original) The method of claim 6, wherein the step of forming the dielectric layer includes depositing silicon oxide.

9. (original) The method of claim 6, wherein the dielectric layer has a thickness of about 10000Å to 15000Å.

10. (original) The method of claim 6, wherein the dielectric layer comprises a dielectric layer with a good gap-filling capability and a dielectric passivation layer.

11. (original) The method of claim 6, wherein the step of removing the portion of the polysilicon above the dielectric layer and the step of removing a portion of the dielectric layer includes chemical-mechanical polishing.

12. (currently amended) A method of forming a contact plug in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a silicon nitride dielectric liner layer conformal to a surface profile of the substrate and the said first and second gates;

forming a silicon oxide dielectric layer over the substrate;

patterning the silicon oxide layer using the silicon nitride dielectric liner layer as an etch stop and the silicon nitride layer without planarizing the silicon oxide dielectric liner layer to form a self-aligned contact window that exposes a surface of the substrate between the said first and second gates, wherein a dimension of the contact window formed in the silicon oxide dielectric layer and the silicon nitride dielectric liner layer is greater than a distance between the sidewall spacers of the first gate and the second gate;

forming a polysilicon layer over the dielectric layer and filling the self-aligned contact window;

performing chemical-mechanical polishing to remove a portion of the polysilicon layer lying above the silicon oxide layer and a portion of the silicon oxide layer so that the landed plug is formed inside the self-aligned contact window.

13. (original) The method of claim 12, wherein the silicon oxide layer has a thickness of about 10000Å to 15000Å.

14. (original) The method of claim 12, wherein the silicon oxide layer comprises a silicon oxide layer that has a good gap-filling capability and a silicon oxide passivation layer.

15. (currently amended) A method of forming a contact opening in a semiconductor device comprising at least a first gate and a second gate, with first sidewall spacers, over a substrate, and a thin liner ~~oxide~~ dielectric layer disposed conformal to the surface profile of the substrate and the said first and second gates, the method comprising the steps of:

forming a dielectric layer over the semiconductor device; and

patterning the dielectric layer and the dielectric liner layer without planarizing the dielectric layer to form a self-aligned contact window between the said first and second gates, wherein a dimension of the contact window at a top is greater than a distance between the sidwall spacers of the first gate and the second gate, and the dielectric liner layer is converted into second sidewall spacers for the first gate and the second gate.

16. (currently amended) The method of claim 15, wherein ~~the step of forming~~ the dielectric liner layer is formed by ~~includes~~ depositing silicon nitride.

17. (original) The method of claim 15, wherein the step of forming the dielectric layer includes depositing silicon oxide.

18. (original) The method of claim 15, wherein the dielectric layer has a thickness of about 10000Å to 15000Å.

19. (original) The method of claim 15, wherein the dielectric layer comprises a dielectric layer with a good gap-filling capability and a dielectric passivation layer.